Amendments to the Claim of Priority:

Please add the following paragraph on page 1 following the title:

This application is a Continuation of Application No. 09/541,140, filed March 31, 2000, which issued to Patent No. 6,621,760 B1 on September 16, 2003.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1-25. (Canceled)

26. (New) An apparatus comprising:

first logic to generate a write strobe signal that is used to latch output data into a memory unit, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the output data;

second logic to delay a first receive clock signal by a first delay period to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit; and

third logic to align the edge transition of the write strobe signal and the data window.

27. (New) The apparatus of claim 26 wherein the memory unit comprises one or more DDR-SDRAM devices.

28. (New) The apparatus of claim 26 wherein the second logic delays the first receive clock signal using a delay locked loop (DLL) circuit.

29. (New) The apparatus of claim 26 wherein the third logic aligns the edge transition of the write strobe signal and the data window corresponding to the output data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

30. (New) The apparatus of claim 29 wherein the third logic comprises:

first and second latching devices to latch the output data in response to transitions of a first and a second clock signal, respectively, the first and second clock signals being phase

shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

third and fourth latching devices to latch the write strobe signal in response to transitions of a third and a fourth clock signal, respectively, the third and fourth clock signals being phase shifted by one half of the clock period.

31. (New) The apparatus of claim 30 wherein the first, second, third, and fourth clock signals are derived from a system clock signal using a phase locked loop (PLL) circuit.

32. (New) The apparatus of claim 28 wherein the DLL circuit is programmable via a register.

33. (New) The apparatus of claim 32 wherein the first delay period corresponds to a value stored in the register.

34. (New) The apparatus of claim 26 further comprising fourth logic to delay a second receive clock signal by the first delay period.

35. (New) The apparatus of claim 34 wherein the fourth logic delays the second receive clock signal by the first delay period by using a DLL circuit to generate a second delayed receive clock signal, the second delayed receive clock signal being used to latch incoming data from the memory unit.

36. (New) A method comprising:

generating a write strobe signal that is used to latch output data into a memory unit, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the output data;

delaying a first receive clock signal by a first delay period to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit; and

aligning the edge transition of the write strobe signal and the data window.

37. (New) The method of claim 36 wherein the memory unit comprises one or more DDR-SDRAM devices.

38. (New) The method of claim 36 wherein the first receive clock signal is delayed using a delay locked loop (DLL) circuit.

39. (New) The method of claim 36 wherein the edge transition of the write strobe signal and the data window are aligned corresponding to the output data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

40. (New) The method of claim 39 wherein aligning the edge transition of the write strobe signal and the data window further comprises:

latching the output data in response to transitions of a first and a second clock signal, respectively, the first and second clock signals being phase shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

latching the write strobe signal in response to transitions of a third and a fourth clock signal, respectively, the third and fourth clock signals being phase shifted by one half of the clock period.

41. (New) The method of claim 40 wherein the first, second, third, and fourth clock signals are derived from a system clock signal using a phase locked loop (PLL) circuit.

42. (New) The method of claim 38 wherein the DLL circuit is programmable via a register.

43. (New) The method of claim 42 wherein the first delay period corresponds to a value stored in the register.

44. (New) The method of claim 36 further comprising delaying a second receive clock signal by the first delay period.

45. (New) The method of claim 44 wherein the second receive clock signal is delayed by the first delay period by using a DLL circuit to generate a second delayed receive clock signal, the second delayed receive clock signal being used to latch incoming data from the memory unit.

46. (New) A system comprising:

a memory unit; and

a graphics accelerator coupled to the memory unit including a memory interface to control data transfer between the graphics accelerator and the memory unit, the memory interface comprising:

first logic to generate a write strobe signal that is used to latch output data into a memory unit, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the output data;

second logic to delay a first receive clock signal by a first delay period to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit; and

third logic to align the edge transition of the write strobe signal and the data window.

47. (New) The system of claim 46 wherein the memory unit comprises one or more DDR-SDRAM devices.

48. (New) The system of claim 46 wherein the second logic delays the first receive clock signal using a delay locked loop (DLL) circuit.

49. (New) The system of claim 46 wherein the third logic aligns the edge transition of the write strobe signal and the data window corresponding to the output data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

50. (New) The system of claim 49 wherein the third logic comprises:

first and second latching devices to latch the output data in response to transitions of a first and a second clock signal, respectively, the first and second clock signals being phase shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

third and fourth latching devices to latch the write strobe signal in response to transitions of a third and a fourth clock signal, respectively, the third and fourth clock signals being phase shifted by one half of the clock period.

51. (New) The system of claim 50 wherein the first, second, third, and fourth clock signals are derived from a system clock signal using a phase locked loop (PLL) circuit.

52. (New) The system of claim 48 wherein the DLL circuit is programmable via a register.

53. (New) The system of claim 52 wherein the first delay period corresponds to a value stored in the register.

54. (New) The system of claim 46 further comprising fourth logic to delay a second receive clock signal by the first delay period.

55. (New) The system of claim 54 wherein the fourth logic delays the second receive clock signal by the first delay period by using a DLL circuit to generate a second delayed receive clock signal, the second delayed receive clock signal being used to latch incoming data from the memory unit.